74HC02; 74HCT02

Quad 2-input NOR gate Rev. 6 — 7 April 2020

Product data sheet

1. General description

The 74HC02; 74HCT02 is a quad 2-input NOR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Input levels:
 - For 74HC02: CMOS level
 - For 74HCT02: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
 - HBM JESD22-A114F exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

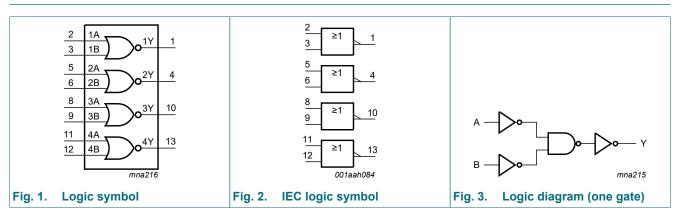
3. Ordering information

Table 1. Ordering information

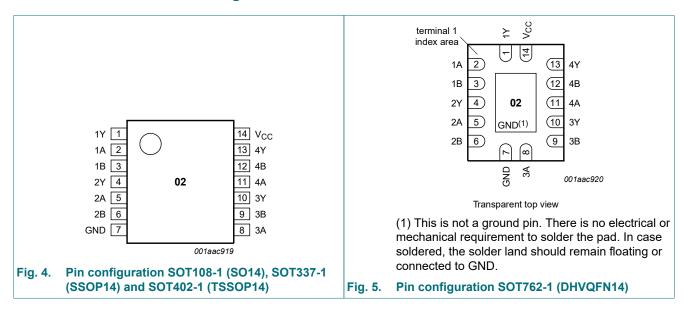
Type number	Package						
	Temperature range	Name	Description	Version			
74HC02D	-40 °C to +125 °C	SO14	······································				
74HCT02D			body width 3.9 mm				
74HC02DB	-40 °C to +125 °C	SSOP14					
74HCT02DB			body width 5.3 mm				
74HC02PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package;	SOT402-1			
74HCT02PW			14 leads; body width 4.4 mm				
74HC02BQ	-40 °C to +125 °C	DHVQFN14 plastic dual in-line compatible thermal		SOT762-1			
74HCT02BQ			enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm				

nexperia

4. Functional diagram



5. Pinning information



5.1. Pinning



Symbol	Pin	Description				
1Y to 4Y	1, 4, 10, 13	data output				
1A to 4A	2, 5, 8, 11	data input				
1B to 4B	3, 6, 9,12	data input				
GND	7	ground (0 V)				
V _{CC}	14	supply voltage				

Table 2. Pin description

74HC_HCT02

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input	Output	
nA	nB	nY
L	L	Н
X	Н	L
Н	X	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{\rm I}$ < -0.5 V or $V_{\rm I}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I _O	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC02		74HCT02			Unit	
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Мах	Min	Max	1
74HC02	1	I				1			1	1
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH}$ or V_{IL}								
output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V	
	I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V	
	I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V	
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2.0	-	20	-	40	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT0	2									-
V _{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA	-	0.15	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5 V$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μA

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Symbol	Symbol Parameter Conditions			25 °C		-40 °C to +85		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Мах	
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	150	540	-	675	-	735	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $C_L = 50 pF$; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C te	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC02								•		
t _{pd}	propagation	nA, nB to nY; see Fig. 6 [1]								
	delay	V _{CC} = 2.0 V	-	25	90	-	115	-	135	ns
		V _{CC} = 4.5 V	-	9	18	-	23	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	7	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	7	15	-	20	-	23	ns
t _t	transition time	see <u>Fig. 6</u> [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; [3] $V_I = GND$ to V_{CC}	-	22	-	-	-	-	-	pF
74HCT02	2					1		•		
t _{pd}	propagation	nA, nB to nY; see Fig. 6 [1]								
	delay	V _{CC} = 4.5 V	-	11	19	-	24	-	29	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 6</u> [2]	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; [3] $V_I = GND$ to V_{CC} - 1.5 V	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} . [2] t_t is the same as t_{THL} and t_{TLH} . [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W): $P_D = C_{PD} x V_{CC}^2 x f_i x N + \sum (C_L x V_{CC}^2 x f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

10.1. Waveforms

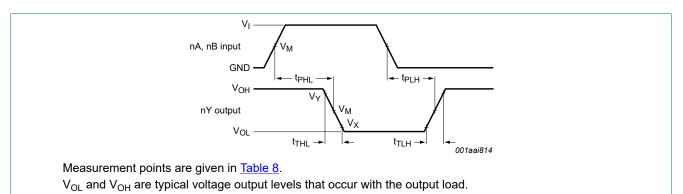
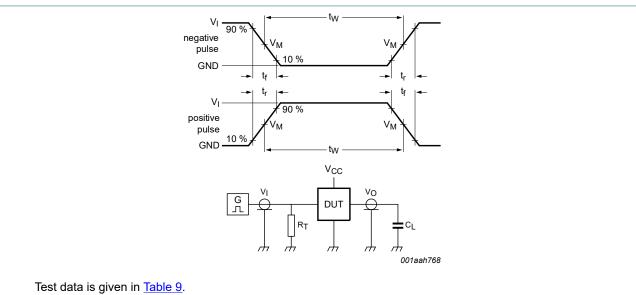


Fig. 6. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output	Output				
	V _M	V _M	V _X	V _Y			
74HC02	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}			
74HCT02	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}			



Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Туре	Input Lo		Load	Test
	VI	t _r , t _f	CL	
74HC02	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT02	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

74HC_HCT02

11. Package outline

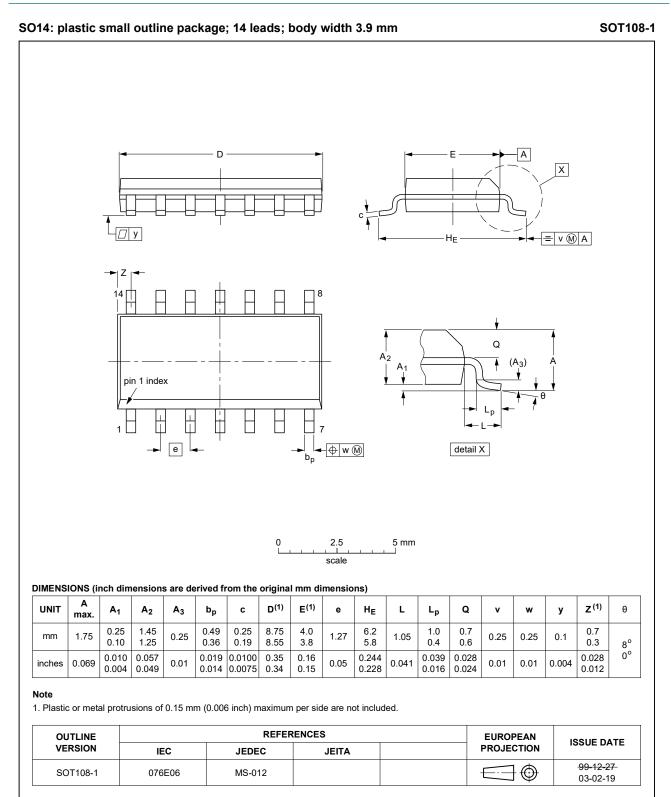


Fig. 8. Package outline SOT108-1 (SO14)

Quad 2-input NOR gate

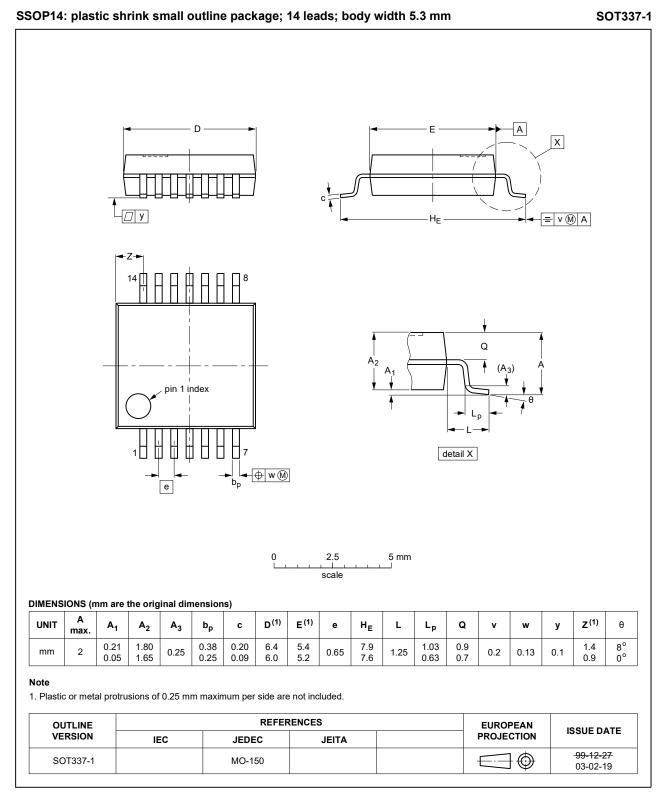


Fig. 9. Package outline SOT337-1 (SSOP14)

Quad 2-input NOR gate

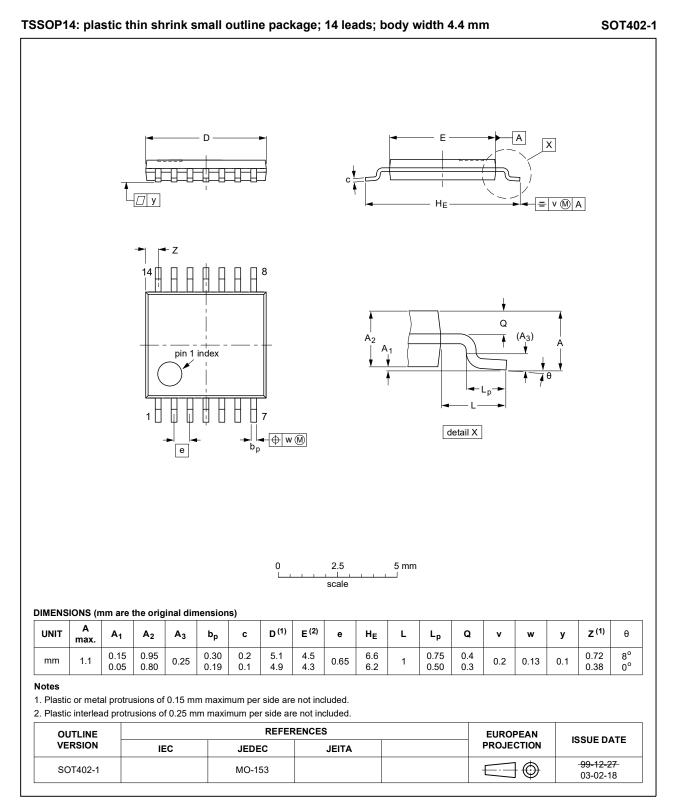


Fig. 10. Package outline SOT402-1 (TSSOP14)

74HC02; 74HCT02

Quad 2-input NOR gate

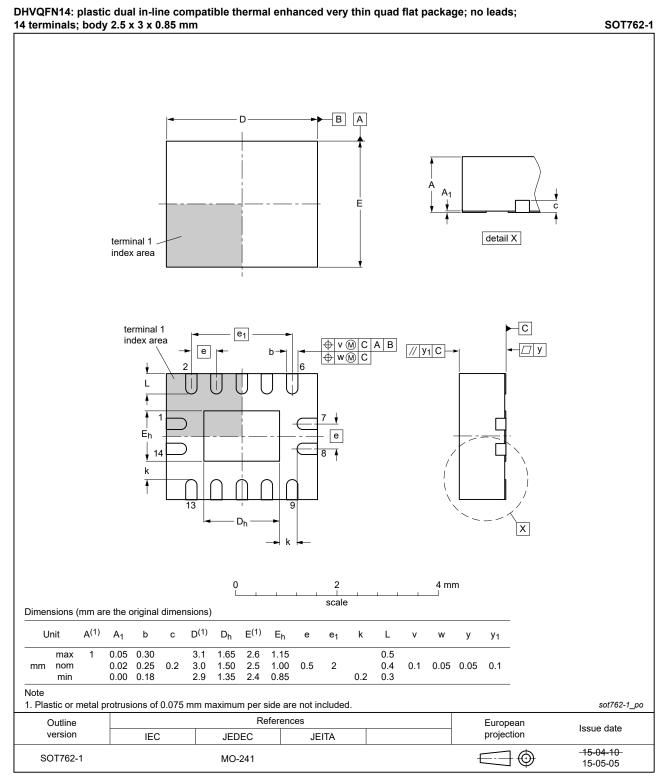


Fig. 11. Package outline SOT762-1 (DHVQFN14)

Product data sheet

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12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74HC_HCT02 v.6	20200407	Product data sheet	-	74HC_HCT02 v.5		
Modifications:	Nexperia. • Legal texts have bee	ta sheet has been redesig n adapted to the new com ues for P _{tot} total power dis	npany name where app	ropriate.		
74HC_HCT02 v.5	20151126	Product data sheet	-	74HC_HCT02 v.4		
Modifications:	Type numbers 74HC	02N and 74HCT02N (SO	T27-1) removed.			
74HC_HCT02 v.4	20120904	Product data sheet	-	74HC_HCT02 v.3		
Modifications:	 Conditions for V_{OH}, I_I 	and I_{CC} updated to the fa	mily specification (erra	ta).		
74HC_HCT02 v.3	20080918	Product data sheet	-	74HC_HCT02_CNV v.2		
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type numbers 74HC02BQ and 74HCT02BQ (DHVQFN14 package) 					
74HC_HCT02_CNV v.2	19970827	Product specification	-	-		

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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